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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/804,608	03/18/2004	Kirsten Renick	501315.01 (30299/US)	9553
7590 Edward W. Bulchis, Esq. DORSEY & WHITNEY LLP Suite 3400 1420 Fifth Avenue Seattle, WA 98101			EXAMINER LEE, CHUN KUAN	
			ART UNIT 2181	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE			MAIL DATE	DELIVERY MODE
3 MONTHS			01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/804,608	Applicant(s) RENICK, KIRSTEN	
	Examiner Chun-Kuan (Mike) Lee	Art Unit 2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-48 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-48 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 October 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 10/31/2006 have been fully considered but they are not persuasive. Objection to the drawings of Figures 1-3 is withdrawn. Objection of claim 21 due to informalities is withdrawn. Currently, claims 1-48 are pending for examination.

2. In regarding to the rejection of independent claims 1, 12, 23, 29, 40 and 44 rejected under 35 U.S.C. § 103(a), applicant appears to argue that the references individually fail to teach the claimed features of applicant's invention, as stated on page 19, 2nd paragraph to page 20 1st paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

The examiner relied on AAPA for most of applicant's claimed limitations, such as AAPA's disclosure of the prior art Figures 1 and 2 in the Drawings and the corresponding disclosure in the Specification, wherein the Drawings and the Specification teaches that the bandwidth are not fully utilized as certain bandwidth are being left empty and unused. The examiner then relied on Caldara for the teaching in

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the optimization of bandwidth utilization by reallocating unused bandwidth for other data transferring; therefore, the combined teaching would obviously further teach the fully utilization of the bandwidth capacity, as each of the unused bandwidth is reallocated to be filled for data transferring. More specifically, the examiner rejected the claimed limitations of independent claims 1 and 29 in detail below:

AAPA teaches a processor-based system, comprising:

a processor (Drawings, Fig. 1, ref. 104) having a processor bus (Drawings, Fig. 1, ref. 106);

a system controller (Drawings, Fig. 1, ref. 110) coupled to the processor bus, the system controller having a peripheral device port (Specification, [006]);

at least one input device (Drawings, Fig. 1, ref. 118) coupled to the peripheral device port of the system controller (Specification, [006]);

at least one output device (Drawings, Fig. 1, ref. 120) coupled to the peripheral device port of the system controller (Specification, [006]);

at least one data storage device (Drawings, Fig. 1, ref. 124) coupled to the peripheral device port of the system controller (Specification, [006]); and

a memory hub controller (Drawings, Fig. 1, ref. 128) coupled to the processor bus;

a plurality of memory modules (Drawings, Fig. 1, ref. 130a-130n) coupled to the memory hub controller by at least one bus (Drawings, Fig. 1, ref. 134), each of the memory modules comprising:

a plurality of memory devices (Drawings, Fig. 1, ref. 148); and

a memory hub (Drawings, Fig. 1, ref. 140), comprising:

a memory controller coupled to the memory devices (Specification, [007]-[0011]), as the received request for data from the memory modules (Drawings, Fig. 1, ref. 130a-130n) must properly identified in order to be routed to the appropriate memory module and the requested data must then be properly returned to the memory hub controller (Drawings, Fig. 1, ref. 128), the memory hub must have the memory controller for implementing such routing control;

at least one receive interface coupled to the memory controller through a bus system (Specification, [007]-[011]), in order to receive the memory request to the memory module, the memory hub must have the interface for receiving the memory request through the bus system; and

at least one transmit interface coupled to the memory controller through the bus system to transmit memory transactions from the memory module to the memory controller (Specification, [007]-[011]), in order to transfer the requested data back, resulted from the memory request, there must be the interface for transmitting the requested data to the next memory controller inside the next memory hub or back to the memory controller hub (Drawings, Fig. 1, ref. 128), depending on where the memory module is located (Specification, [009]),

each transmit interface receiving memory transactions each of which comprises a command header and data having a variable

number of data bits (Drawings, Fig. 2, ref. 162, 164, 166, 168 and Specification, [012]), wherein the number of data bits depends on the number of 32-bit groups of data,

each transmit interface including a data organization system (Drawings, Fig. 2) organizing the command header and data into lane groups (Drawings, Fig. 2, ref. 175-179) each of which includes a plurality of lanes (i.e. eight lanes) each of which contains a plurality of parallel command header bits or parallel data bits (Drawings, Fig. 2, ref. 175-179 and Specification, [012]),

the data organization system (Drawings, Fig. 2) being operable to convert each of the lane groups into a serial stream of the lanes for transmission by the transmit interface (Drawings, Fig. 2, ref. 174), wherein parallel data are serially outputted (Drawings, Fig. 2, ref. 134) , as the conversion is implemented by the parallel to serial converter (Drawings, Fig. 2, ref. 174),

each of the transmitted lanes containing a plurality of parallel command header bits or parallel data bits (Drawings, Fig. 2, ref. 134 and Specification, [012]).

AAPA does not expressly teach the data organization system organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits.

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and transferring the buffered data cells without processing any empty storage location, as available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 5-10 and col. 3, ll. 28-33).

By combining Caldara's buffering the current data cell right after the previously buffered data cell without leaving any empty buffer location into AAPA's data organization system, the resulting combination of the references teaches the processor-based system comprising wherein the data organization system fill all the lanes (i.e. buffers) by buffering the current data cell right after the previously buffered data cell without leaving any empty buffer location, therefore buffering either command header bits or data bits.

The examiner relied on AAPA and Caldara in the similar manner for the rejection of the remaining independent claims 23, 29, 40 and 44, as discussed in detail in the rejections below.

3. In responding to applicant's arguments regarding the independent claims 1, 12, 23, 29, 40 and 44 rejected under 35 U.S.C. § 103(a) that Caldara is nonanalogous art, because Caldara is directed towards the ATM switch managing the traffic flow to a plurality of buses having a plurality of bandwidth and delay requirements, as stated on

page 20, last paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992).

In this case, both AAPA and Caldara are associated with transferring of data through multiplexing, furthermore, Caldara's teaching is reasonably pertinent to the particular problem with which the applicant was concerned, as Caldara teaches the optimization of bandwidth utilization by buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Caldara, Fig. 6) and transferring the buffered data cells without processing any empty storage location (i.e. utilizing all available capacity of the high speed bus), as bandwidth that are not been utilized are dynamically reallocated to be utilized for data transferring for another group (Caldara, col. 3, ll. 5-10 and col. 3, ll. 28-33).

4. In responding to applicant's arguments regarding the independent claims 1, 12, 23, 29, 40 and 44 rejected under 35 U.S.C. § 103(a) that there is no motivation or suggestion for combine Caldara with AAPA, as one skilled in the art would not be motivated to modify an ATM switch system as in the Caldara reference to a

conventional memory hub system for routing memory requests into packets and into a single high speed bus, as stated on page 20, last paragraph to page 21, 1st paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

Caldara provided the motivation to combine with AAPA for the benefit of implementing the data transferring system that is able to dynamically accommodate for changes in the data traffic and bandwidth requirements (Caldara, col. 1, ll. 57-60), therefore optimize the utilization of the high speed bus's bandwidth by utilizing all available bandwidth capacity of the high speed bus (Caldara, col. 3, ll. 5-10 and col. 3, ll. 28-33).

5. In responding to applicant's arguments regarding the independent claims 1 and 29 rejected under 35 U.S.C. § 103(a) that the combined teachings of AAPA and Caldara does not teach or suggest every claimed features, because the combined teaching does not teach the optimization of the bandwidth of a high speed bus by filling a plurality of lane groups to capacity and converts the plurality of lane groups to a serial stream of lanes, as stated on page 21, 3rd paragraph. Applicant's arguments are fully considered, but are not found to be persuasive.

The examiner relied on AAPA for the teaching the transferring of data on a high speed bus to a plurality of lane groups (Drawings, Fig. 2, ref. 175-179) and converts the plurality of lane groups to a serial stream of lanes (Drawings, Fig. 2, ref. 134) (Drawings, Fig. 2); and relies on Caldara for the teaching the optimization of a bus's bandwidth by dynamically reallocation of available unused bandwidth for data transferring (Caldara,

col. 3, ll. 5-10 and col. 3, ll. 28-33); therefore, the resulting combination of the reference teaches the optimization of the high speed bus' bandwidth for transferring of data on the high speed bus, by dynamically reallocating unfilled lanes in the plurality of lane groups for the transferring of data, therefore filling the plurality of lane groups to capacity, and converts the plurality of lane groups to the serial stream of lanes; furthermore, the dynamic reallocation of the unfilled lanes would obviously resulted in the reorganization of the data in order to fill the lane groups completely.

As applicant appears to present similar argument regarding the filling of the plurality of lane groups to the filling of the group (i.e. directed towards claim 12 on page 22, 1st paragraph) and the filling of all the lanes in each lane group (i.e. directed towards claim 23 on page 22, 2nd paragraph); the examiner will also apply similar response to applicant's arguments for claims 12 and 23.

6. In responding to applicant's arguments regarding the independent claim 40 rejected under 35 U.S.C. § 103(a) that the combined teachings of AAPA and Caldara does not teach organizing groups of data by sub-groups and transmitting the data as a serial stream of sub-groups, as stated on page 22, last paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

AAPA teaches the organization of data by subgroups (Drawings, Fig. 2, ref. 162, 164, 166, 168, 175-179) and transmitting the data as a serial stream of sub-groups (Drawings, Fig. 2, ref. 134).

7. In responding to each of applicant's arguments regarding the independent claims 1, 12, 23, 29 and 40 rejected under 35 U.S.C. § 103(a) that there is not motivation or suggestion to combine Caldara with AAPA, as stated on page 21, 3rd paragraph to page 22, last paragraph. Applicant's arguments have fully been considered, but are not found to be persuasive.

Please view the examiner's response pertaining to the motivation for combination of the references in detail above.

8. In responding to all applicant's arguments, the examiner maintains his position and rejection of record in detail below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1-4, 6, 10-15, 17, 21-25, 28-32, 34, and 38-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Caldara et al. (US Patent 5,748,629).

10. As per claims 1 and 29, AAPA teaches a processor-based system, comprising:

a processor (Drawings, Fig. 1, ref. 104) having a processor bus (Drawings, Fig. 1, ref. 106);

a system controller (Drawings, Fig. 1, ref. 110) coupled to the processor bus, the system controller having a peripheral device port (Specification, [006]);

at least one input device (Drawings, Fig. 1, ref. 118) coupled to the peripheral device port of the system controller (Specification, [006]);

at least one output device (Drawings, Fig. 1, ref. 120) coupled to the peripheral device port of the system controller (Specification, [006]);

at least one data storage device (Drawings, Fig. 1, ref. 124) coupled to the peripheral device port of the system controller (Specification, [006]); and

a memory hub controller (Drawings, Fig. 1, ref. 128) coupled to the processor bus;

a plurality of memory modules (Drawings, Fig. 1, ref. 130a-130n) coupled to the memory hub controller by at least one bus (Drawings, Fig. 1, ref. 134), each of the memory modules comprising:

a plurality of memory devices (Drawings, Fig. 1, ref. 148); and

a memory hub (Drawings, Fig. 1, ref. 140), comprising:

a memory controller coupled to the memory devices (Specification, [007]-[0011]), as the received request for data from the memory modules (Drawings, Fig. 1, ref. 130a-130n) must properly identified in order to be routed to the appropriate memory module and the requested data must then be properly returned to the memory hub controller (Drawings, Fig. 1,

ref. 128), the memory hub must have the memory controller for implementing such routing control;

at least one receive interface coupled to the memory controller through a bus system (Specification, [007]-[011]), in order to receive the memory request to the memory module, the memory hub must have the interface for receiving the memory request through the bus system; and

at least one transmit interface coupled to the memory controller through the bus system to transmit memory transactions from the memory module to the memory controller (Specification, [007]-[011]), in order to transfer the requested data back, resulted from the memory request, there must be the interface for transmitting the requested data to the next memory controller inside the next memory hub or back to the memory controller hub (Drawings, Fig. 1, ref. 128), depending on where the memory module is located (Specification, [009]),

each transmit interface receiving memory transactions each of which comprises a command header and data having a variable number of data bits (Drawings, Fig. 2, ref. 162, 164, 166, 168 and Specification, [012]), wherein the number of data bits depends on the number of 32-bit groups of data,

each transmit interface including a data organization system (Drawings, Fig. 2) organizing the command header and data into lane groups (Drawings, Fig. 2, ref. 175-179) each of which includes

a plurality of lanes (i.e. eight lanes) each of which contains a plurality of parallel command header bits or parallel data bits (Drawings, Fig. 2, ref. 175-179 and Specification, [012]),

the data organization system (Drawings, Fig. 2) being operable to convert each of the lane groups into a serial stream of the lanes for transmission by the transmit interface (Drawings, Fig. 2, ref. 174), wherein parallel data are serially outputted (Drawings, Fig. 2, ref. 134) , as the conversion is implemented by the parallel to serial converter (Drawings, Fig. 2, ref. 174),

each of the transmitted lanes containing a plurality of parallel command header bits or parallel data bits (Drawings, Fig. 2, ref. 134 and Specification, [012]).

AAPA does not expressly teach the data organization system organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits.

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and transferring the buffered data cells without processing any empty storage location, as available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 5-10 and col. 3, ll. 28-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Caldara's buffering the current data cell right after the previously buffered data cell without leaving any empty buffer location into AAPA's data organization system. The resulting combination of the references teaches the processor-based system comprising wherein the data organization system fill all the lanes (i.e. buffers) by buffering the current data cell right after the previously buffered data cell without leaving any empty buffer location, therefore buffering either command header bits or data bits.

Therefore, it would have been obvious to combine Caldara with AAPA for the benefit of implementing data transferring system that is able to dynamically accommodate for changes in the data traffic and bandwidth requirements (Caldara, col. 1, ll. 57-60).

11. As per claims 2 and 30, AAPA and Caldara teach all the limitations of claims 1 and 29 as discussed above, where AAPA further teaches the processor-based system comprising wherein each of the lane groups comprise eight lanes (AAPA, Drawings, Fig. 2, ref. 175-179).

12. As per claims 3 and 31 AAPA and Caldara teach all the limitations of claims 1 and 29 as discussed above, where AAPA further teaches the processor-based system comprising wherein each of the lanes comprise 32 parallel bits of command header or data (AAPA, Specification, [012]).

13. As per claim 4 and 32, AAPA and Caldara teach all the limitations of claims 1 and 29 as discussed above, where both further teach the processor-based system comprising wherein the bus system comprises:

a downstream bus (AAPA, Drawings, Fig. 1, ref. 134) for coupling memory transactions transmitted by the memory modules away from the memory controller (AAPA, Specification, [009]) and

an upstream bus for coupling memory transactions transmitted by the memory modules toward the memory controller (AAPA, Specification, [009]), and

wherein the transmit interface comprises an upstream transmit interface coupled to the upstream bus and a downstream transmit interface coupled to the downstream bus (AAPA, Specification, [007]-[012] and Caldara, Fig. 1 ref, 20, 22),

each of the upstream and downstream transmit interfaces including a respective one of the data organization systems (Caldara, Fig. 1 ref, 20, 22), wherein each input or output port have the corresponding data processing system.

14. As per claim 6 and 34, AAPA and Caldara teach all the limitations of claims 1 and 29 as discussed above, where both further teach the processor-based system comprising wherein the data organization system comprises:

a data organization unit (AAPA, Drawings, Fig. 2, ref. 160) organizing the command header and data into lane groups each of which includes a plurality of lanes containing either a command header or data (AAPA, Drawings, Fig. 2, ref. 175-179), the

data organization unit organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits (Caldara, Fig. 6; col. 3, ll. 4-9 and col. 3, ll.28-33); and

a parallel-to-serial converter (AAPA, Drawings, Fig. 2, ref. 174) converting each of the lane groups into a serial stream of the lanes for transmission by the transmit interface (AAPA, Specification, [012]).

15. As per claims 10 and 38, AAPA and Caldara teach all the limitations of claims 1 and 34 as discussed above, where both further teach the processor-based system comprising wherein the data organization system comprises wherein the data organization unit is configurable to vary the number of lanes in each lane groups that are coupled from the data organization during each cycle of a clock signal (AAPA, Specification, [010] and Caldara, col. 6, ll. 11-17), as the bandwidth can be dynamically reallocated, therefore the number of lanes can be configured to be varied.

16. As per claims 11 and 39, AAPA and Caldara teach all the limitations of claims 1 and 29 as discussed above, where AAPA further teaches the processor-based system comprising wherein the command header and data for each of the transactions comprise a memory packet (AAPA, Specification, [008]).

17. As per claim 12, AAPA teaches a memory module, comprising:
a plurality of memory devices (Drawings, Fig. 1, ref. 148); and

a memory hub (Drawings, Fig. 1, ref. 140), comprising:

a memory controller coupled to the memory devices (Specification, [007]-[0011]), as the received request for data from the memory modules (Drawings, Fig. 1, ref. 130a-130n) must properly identified in order to be routed to the appropriate memory module and the requested data must then be properly returned to the memory hub controller (Drawings, Fig. 1, ref. 128), the memory hub must have the memory controller for implementing such routing control;

at least one receive interface coupled to the memory controller (Specification, [007]-[011]), in order to receive the memory request to the memory module, the memory hub must have the interface for receiving the memory request through the bus system; and

at least one transmit interface coupled to the memory controller to transmit memory transactions from the memory module (Specification, [007]-[011]), in order to transfer the requested data back, resulted from the memory request, there must be the interface for transmitting the requested data to the next memory controller inside the next memory hub or back to the memory controller hub (Drawings, Fig. 1, ref. 128), depending on where the memory module is located (Specification, [009]),

each transmit interface receiving memory transactions each of which comprises a command header and data having a variable number of data bits (Drawings, Fig. 2, ref. 162, 164, 166, 168 and Specification,

[012]), wherein the number of data bits depends on the number of 32-bit groups of data,

each transmit interface including a data organization system (Drawings, Fig. 2) that is operable to organize the command header and data into groups (Drawings, Fig. 2, ref. 175-179) each of which contains a predetermined number of sub-groups (i.e. eight sub-groups) of a predetermined size (i.e. 32-bits) (Drawings, Fig. 2, ref. 175-179 and Specification, [012]),

each of the sub-groups containing a plurality of parallel command header bits or data bits (Drawings, Fig. 2, ref. 134 and Specification, [012]),

the data organization system further being operable to output each group of data as a serial stream of the sub-groups (Drawings, Fig. 2, ref. 134), as parallel data is converted to serial data by the parallel to serial data converter (Drawings, Fig. 2, ref. 174).

AAPA does not expressly teach that each sub-group containing data for a first transaction being immediately followed by a sub-group containing either additional data for the first transaction or the command header for a second transaction so that each group is filled with sub-groups containing either command header bits or data bits,

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and

transferring the buffered data cells without processing any empty storage location, as available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 4-9 and col. 3, ll.28-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Caldara's the storing of data cells without leaving any empty storage cells between the previously stored data cell and the currently stored data cell into AAPA's memory module.

Therefore, it would have been obvious to combine Caldara with AAPA for reason stated above in claims 1 and 29.

18. As per claim 13, AAPA and Caldara teach all the limitations of claim 12 as discussed above, where AAPA further teaches the memory module comprising wherein each of the groups comprise eight sub-groups (AAPA, Drawings, Fig. 2, ref. 175-179).

19. As per claim 14, AAPA and Caldara teach all the limitations of claim 12 as discussed above, where AAPA further teaches the memory module comprising wherein each of the sub-groups comprise 32 parallel bits of command header or data (AAPA, Specification, [012]).

20. As per claim 15, AAPA and Caldara teach all the limitations of claim 12 as discussed above, where both further teach the memory module comprising wherein the at least one transmit interface comprises an upstream transmit interface and a

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downstream transmit interface (AAPA, Specification, [007]-[012] and Caldara, Fig. 1 ref, 20, 22) each of which comprises the data organization system (Caldara, Fig. 1 ref, 20, 22), wherein each input or output port have the corresponding data processing system.

21. As per claim 17, AAPA and Caldara teach all the limitations of claim 12 as discussed above, where both further teach the memory module comprising:

a data organization unit (AAPA, Drawings, Fig. 2, ref. 160) organizing the command header and data into groups each of which includes a plurality of the sub-groups containing either a command header or data (AAPA, Drawings, Fig. 2, ref. 175-179), the data organization unit organizing the groups so that all of the sub-groups in each group are filled with either command header bits or data bits (Caldara, Fig. 6; col. 3, ll. 4-9 and col. 3, ll.28-33); and

a parallel-to-serial converter (AAPA, Drawings, Fig. 2, ref. 174) converting each of the groups into a serial stream of the sub-groups for transmission by the transmit interface (AAPA, Specification, [012]).

22. As per claim 21, AAPA and Caldara teach all the limitations of claim 17 as discussed above, where both further teach the memory module comprising wherein the data organization unit is configurable to vary the number of sub-groups in each groups that are coupled from the data organization during each cycle of a clock signal (AAPA, Specification, [010] and Caldara, col. 6, ll. 11-17), as the bandwidth can be dynamically reallocated, therefore the number of lanes can be configured to be varied.

23. As per claim 22, AAPA and Caldara teach all the limitations of claim 12 as discussed above, where AAPA further teaches the memory module comprising wherein the command header and data for each of the transactions comprise a memory packet (AAPA, Specification, [008]).

24. As per claim 23, AAPA teaches a data organization system (Fig. 2), comprising:
a data organization unit (Drawings, Fig. 2, ref. 160) organizing a command header and data for each of a plurality of memory transaction into lane groups each of which includes a plurality of lanes each of which contains a plurality of parallel command header bits or parallel data bits (Drawings, Fig. 2, ref. 175-179 and Specification, [012]); and

a parallel-to-serial converter (Drawings, Fig. 2, ref. 174) converting each of the lane groups into a serial stream of the lanes each of which contains a plurality of parallel command header bits or parallel data bits (AAPA, Specification, [012]).

AAPA does not teach the data organization system comprising wherein the data organization unit organizing the lane groups so that all of the lanes in each lane group are filled with either command header bits or data bits

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and transferring the buffered data cells without processing any empty storage location, as

available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 4-9 and col. 3, ll.28-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Caldara's the storing of data cells without leaving any empty storage cells between the previously stored data cell and the currently stored data cell into AAPA's data organization system.

Therefore, it would have been obvious to combine Caldara with AAPA for reason stated above in claims 1 and 29.

25. As per claim 24, AAPA and Caldara teach all the limitations of claim 23 as discussed above, where AAPA further teaches the data organization system comprising wherein each of the lane groups comprise eight lanes (AAPA, Drawings, Fig. 2, ref. 175-179).

26. As per claim 25, AAPA and Caldara teach all the limitations of claim 23 as discussed above, where AAPA further teaches the data organization system comprising wherein each of the lanes comprise 32 parallel bits of command header or data (AAPA, Specification, [012]).

27. As per claim 28, AAPA and Caldara teach all the limitations of claim 23 as discussed above, where both further teach the data organization system comprising wherein the data organization unit is configurable to vary the number of lanes in each

lane groups that are coupled from the data organization during each cycle of a clock signal (AAPA, Specification, [010] and Caldara, col. 6, ll. 11-17), as the bandwidth can be dynamically reallocated, therefore the number of lanes can be configured to be varied.

28. As per claim 40, AAPA teaches a method of transmitting memory transactions each of which comprises a command header and a variable amount of data (Drawings, Fig. 2 ref. 162-168), the method comprising:

organizing the command header and data into groups each of which contains a predetermined number of sub-groups (i.e. eight sub-groups) of a predetermined size (i.e. 32-bit) (Drawings, Fig. 2 and Specification, [010]-[011]),

each of the sub-groups containing a plurality of parallel command header bits or data bits (Specification, [012]); and

transmitting each group of data as a serial stream of the sub-groups (Drawings, Fig. 2, ref. 134) each of which includes the plurality of parallel command header bits or data bits (Specification, [012]), as parallel data is converted to serial data by the parallel to serial data converter (Drawings, Fig. 2, ref. 174).

AAPA does not expressly teach the method comprising wherein each sub-group containing data for a first transaction being immediately followed by a sub-group containing either additional data for the first transaction or the command header for a second transaction so that each group is filled with sub-groups containing either command header bits or data bits.

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and transferring the buffered data cells without processing any empty storage location, as available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 4-9 and col. 3, ll.28-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Caldara's the storing of data cells without leaving any empty storage cells between the previously stored data cell and the currently stored data cell into AAPA's method of transmitting memory transactions.

Therefore, it would have been obvious to combine Caldara with AAPA for reason stated above in claims 1 and 29.

29. As per claim 41, AAPA and Caldara teach all the limitations of claim 40 as discussed above, where AAPA further teaches the method comprising wherein the act of organizing the command header and data into groups comprises organizing the command header and data into groups each of which contains eight sub-groups (AAPA, Drawings, Fig. 2, ref. 175-179).

30. As per claim 42, AAPA and Caldara teach all the limitations of claim 40 as discussed above, where AAPA further teaches the method comprising wherein the act of organizing the command header and data into groups containing a predetermined

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number of sub-groups comprises the command header and data so that each sub-group comprises 32 parallel bits of command header or data (AAPA, Specification, [012]).

31. As per claim 43, AAPA and Caldara teach all the limitations of claim 40 as discussed above, where Caldara further teaches the method further comprising varying the quantity of sub-groups in each group (Caldara, col. 6, ll. 11-17), as the bandwidth can be dynamically reallocated, therefore the number of sub-groups can be configured to be varied.

32. As per claim 44, AAPA teaches a method of transmitting memory transactions each of which comprises a command header and a variable amount of data (Drawings, Fig. 2, ref. 162-168), the method comprising:

organizing the command header and data into lane groups (Drawings, Fig. 2, ref. 175-179) each of which contains a plurality of lanes of a predetermined size (i.e. eight lanes) (Drawings, Fig. 2, ref. 175-179),

each of the lanes containing a plurality of parallel command header bits or data bits (Specification, [012]).

AAPA does not expressly teach the method comprising wherein the lane groups being organizing so that all of the lanes in each lane group are filled with either command header bits or data bits.

Caldara teaches a data transferring system and method comprising buffering data cells into a plurality of queues without leaving any empty storage locations between the previously stored data cell and the currently stored data cell (Fig. 6) and transferring the buffered data cells without processing any empty storage location, as available bandwidth is dynamically reallocated for the transferring another data cell (col. 3, ll. 4-9 and col. 3, ll.28-33).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Caldara's the storing of data cells without leaving any empty storage cells between the previously stored data cell and the currently stored data cell into AAPA's method of transmitting memory transactions.

Therefore, it would have been obvious to combine Caldara with AAPA for reason stated above in claims 1 and 29.

33. As per claim 45, AAPA and Caldara teach all the limitations of claim 44 as discussed above, where AAPA further teaches the method further comprising converting each of the lane groups into a serial stream of the lanes (AAPA, Drawings, Fig. 2, ref. 134) each of which contains a plurality of parallel command header bits or parallel data bits (AAPA, Specification, [012]).

34. As per claim 46, AAPA and Caldara teach all the limitations of claim 44 as discussed above, where AAPA further teaches the method comprising wherein the act of organizing the command header and data into lane groups comprises organizing the

command header and data into lane groups each of which contains eight lanes (AAPA, Drawings, Fig. 2, ref. 175-179).

35. As per claim 47, AAPA and Caldara teach all the limitations of claim 44 as discussed above, where AAPA further teaches the method comprising wherein the act of organizing the command header and data into lane groups each of which contains a predetermined number of lanes comprises organizing the command header and data so that each lane comprises 32 parallel bits of command header or data (AAPA, Specification, [012]).

36. As per claim 48, AAPA and Caldara teach all the limitations of claim 44 as discussed above, where AAPA further teaches the method further comprising varying the number of lanes in each lane group (Caldara, col. 6, ll. 11-17), as the bandwidth can be dynamically reallocated, therefore the number of sub-groups can be configured to be varied.

37. Claims 5, 7-9, 16, 18-20, 26-27, 33 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) and Caldara et al. (US Patent 5,748,629), and in view of Epps et al. (US Patent (6,778,546)).

38. As per claims 5, 7, 33 and 35, AAPA and Caldara teach all the limitation of claim 1, 6, 29 and 34 as discussed above.

AAPA and Caldara does not expressly teach the processor-based system comprising:

wherein the memory devices comprise dynamic random access memory devices;

wherein the data organization unit comprises:

a data buffer storing respective data for a plurality of the transactions, the data for each of the transactions being selectively passed from the data buffer; and

a command queue storing respective command headers for a plurality of the transactions, the command header for each of the transactions being selectively passed from the command queue with the data for the corresponding transaction being passed from the data buffer.

Epps teaches a system and a method comprising:

a memory device comprising a SDRAM (col. 25, ll. 46-51), wherein the SDRAM is a type of DRAM (dynamic random access memory);

a header queue (Fig. 3, ref. 320), buffering the header of the data block (col. 6, ll. 1-12);

a tail queue (Fig. 3, ref. 330), buffering the tail of the data block (col. 6, ll. 1-12); and

wherein the header and tail are selectively transferred through a switch (Fig. 2-3 ref. 220; Fig. 3, ref. 470 and col. 7, ll. 13-20).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Epps' SDRAM, header buffer and tail buffer into AAPA

and Caldara's processor-based system. The resulting combination of the references teaches processor-based system further comprising:

the memory devices comprise SDRAM;

the header queue buffering the command headers;

the tail queue buffering the data; and

wherein the command header and the data are selectively transferred from the queues by the switch.

Therefore, it would have been obvious to combine Epps with AAPA and Caldara for the benefit of providing a flexible transferring system with ultra-high throughput (Epps, col. 3, ll. 1-10).

39. As per claims 8 and 36, AAPA, Caldara and Epps teach all the limitations of claims 7 and 35 as discussed above, where Caldara and Epps further teach the processor-based system comprising:

a multiplexer (Epps, Fig. 3, ref. 470) coupled to receive the data stored in the data buffer (Epps, Fig. 3, ref. 330) for each of the transactions and the command headers stored in the command queue (Epps, Fig. 3, ref. 320) for each of the transactions, the multiplexer being operable to couple the data for each of the transactions and the command header for each of the transactions to an output port responsive to multiplexer control signals (Epps, Fig. 11; col. 7, ll. 13-20 and col. 15, ll. 8-21), wherein the multiplexer control signals is provided by the MUX control block in the Transfer MUX block (Epps, Fig. 11, ref. 470);

an arbitration unit (Caldara, To Switch Port Processor (TSPP) Fig. 6 and Epps, the MUX control block in the Transfer MUX block 470 of Fig. 11) coupled to at least one of the data buffer and the command queue to receive information indicative of the data and command headers for the transactions stored in the data buffer and command queue (Caldara, col. 2, ll. 57-67), as priority associated with the data is received, respectively, the arbitration unit being operable to generate the control signals responsive to the information indicative of the data and command headers to cause the multiplexer to couple a lane group of either data or a command header and data for at least one of the transactions to the output port of the multiplexer (Fig. 11), as the MUX Control provide the control signal, base on the priority of the data, informing the multiplexer which buffered data cells to output.

40. As per claims 9 and 37, AAPA, Caldara and Epps teach all the limitations of claims 8 and 36 as discussed above, where AAPA further teaches the processor-based system further comprising:

a parallel-to-serial converter (AAPA, Drawings, Fig. 2, ref. 174) coupled to the output port of the multiplexer, the parallel-to-serial converter being operative to convert the lane group at the output port of the multiplexer into a serial stream of the lanes (AAPA, Drawings, Fig. 2, ref. 134 and Specification, [012]).

41. Claims 16 and 18-20 repeat the limitations of claims 5 and 7-9 and are therefore rejected accordingly.

42. Claims 26-27 repeat the limitations of claims 7-8 and are therefore rejected accordingly.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

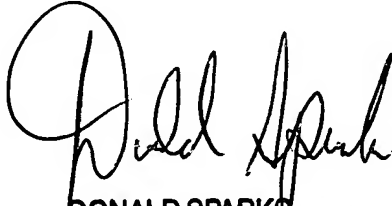
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.K.L.
01/10/2007



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